

## Fixing Assura for DRC and LVS (A mountain 🏔️ to climb!)

### 1. Task 1: Making Assura show up

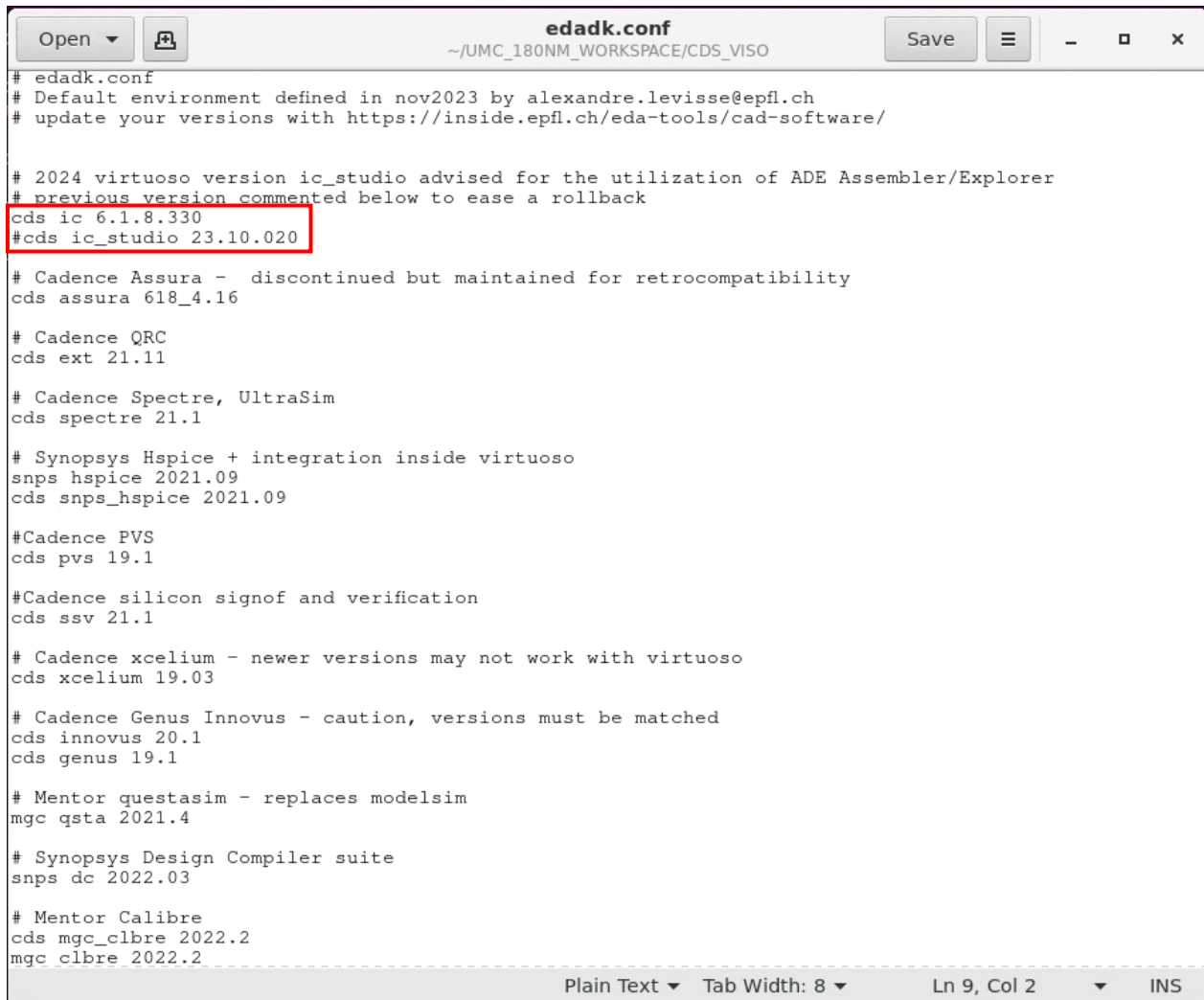
By default, Assura does not show up in the latest version of Cadence Virtuoso (ic\_studio 23.10.020). So, we will revert to an older version of virtuoso for this lab. To do this, close all your existing cadence virtuoso windows (do not disconnect from the **jed** machines though) and go to **UMC\_180NM\_WORKSPACE/CDS\_VISO** folder and open the **edadk.conf** file as shown below:

```
ttharakan@jed2:~  
EDARHEL7[ttharakan@jst007 ~]$ cd ~/UMC_180NM_WORKSPACE/CDS_VISO  
EDARHEL7[ttharakan@jst007 CDS_VISO]$ pwd  
/home/ttharakan/UMC_180NM_WORKSPACE/CDS_VISO  
EDARHEL7[ttharakan@jst007 CDS_VISO]$ gedit edadk.conf &  
[4] 1990863
```

In the edadk.conf file (shown below), you will notice that “cds ic 6.1.8.330” (older version of cadence virtuoso) is commented out and “cds ic\_studio 23.10.020” (newer version of cadence virtuoso) is being used. We will comment out the newer version and use the older version for this TP. Don’t worry - you can continue to use the older version for all your TPs and homework 😊.

```
edadk.conf  
~/UMC_180NM_WORKSPACE/CDS_VISO  
Save  
# edadk.conf  
# Default environment defined in nov2023 by alexandre.levisse@epfl.ch  
# update your versions with https://inside.epfl.ch/eda-tools/cad-software/  
  
# 2024 virtuoso version ic_studio advised for the utilization of ADE Assembler/Explorer  
# previous version commented below to ease a rollback  
#cds ic 6.1.8.330  
cds ic_studio 23.10.020  
  
# Cadence Assura - discontinued but maintained for retrocompatibility  
cds assura 618_4.16  
  
# Cadence QRC  
cds ext 21.11  
  
# Cadence Spectre, UltraSim  
cds spectre 21.1  
  
# Synopsys Hspice + integration inside virtuoso  
snps hspice 2021.09  
cds snps_hspice 2021.09  
  
#Cadence PVS  
cds pvs 19.1  
  
#Cadence silicon signof and verification  
cds ssv 21.1  
  
# Cadence xcelium - newer versions may not work with virtuoso  
cds xcelium 19.03  
  
# Cadence Genus Innovus - caution, versions must be matched  
cds innovus 20.1  
cds genus 19.1  
  
# Mentor questasim - replaces modelsim  
mgc qsta 2021.4  
  
# Synopsys Design Compiler suite  
snps dc 2022.03  
  
# Mentor Calibre  
cds mgc_clbre 2022.2  
mgc clbre 2022.2  
  
Plain Text Tab Width: 8 Ln 11, Col 46 INS
```

After making this change, your edadk.conf file should look something like this:



```
# edadk.conf
# Default environment defined in nov2023 by alexandre.levisse@epfl.ch
# update your versions with https://inside.epfl.ch/eda-tools/cad-software/

# 2024 virtuoso version ic_studio advised for the utilization of ADE Assembler/Explorer
# previous version commented below to ease a rollback
cds ic 6.1.8.330
#cds ic_studio 23.10.020

# Cadence Assura - discontinued but maintained for retrocompatibility
cds assura 618_4.16

# Cadence QRC
cds ext 21.11

# Cadence Spectre, UltraSim
cds spectre 21.1

# Synopsys Hspice + integration inside virtuoso
snps hspice 2021.09
cds snps_hspice 2021.09

#Cadence PVS
cds pvs 19.1

#Cadence silicon signof and verification
cds ssv 21.1

# Cadence xcelium - newer versions may not work with virtuoso
cds xcelium 19.03

# Cadence Genus Innovus - caution, versions must be matched
cds innovus 20.1
cds genus 19.1

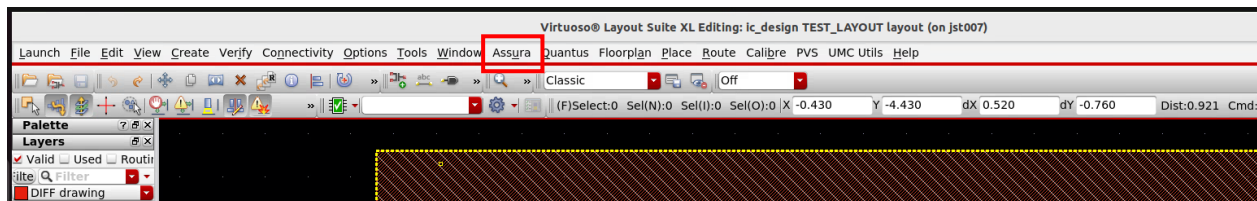
# Mentor questasim - replaces modelsim
mgc qsta 2021.4

# Synopsys Design Compiler suite
snps dc 2022.03

# Mentor Calibre
cds mgc_clbre 2022.2
mgc clbre 2022.2
```

Save the changes by hitting **Ctrl+S** and then close the “edadk.conf” file.

Now, open virtuoso and in the layout window, you should be able to find Assura.

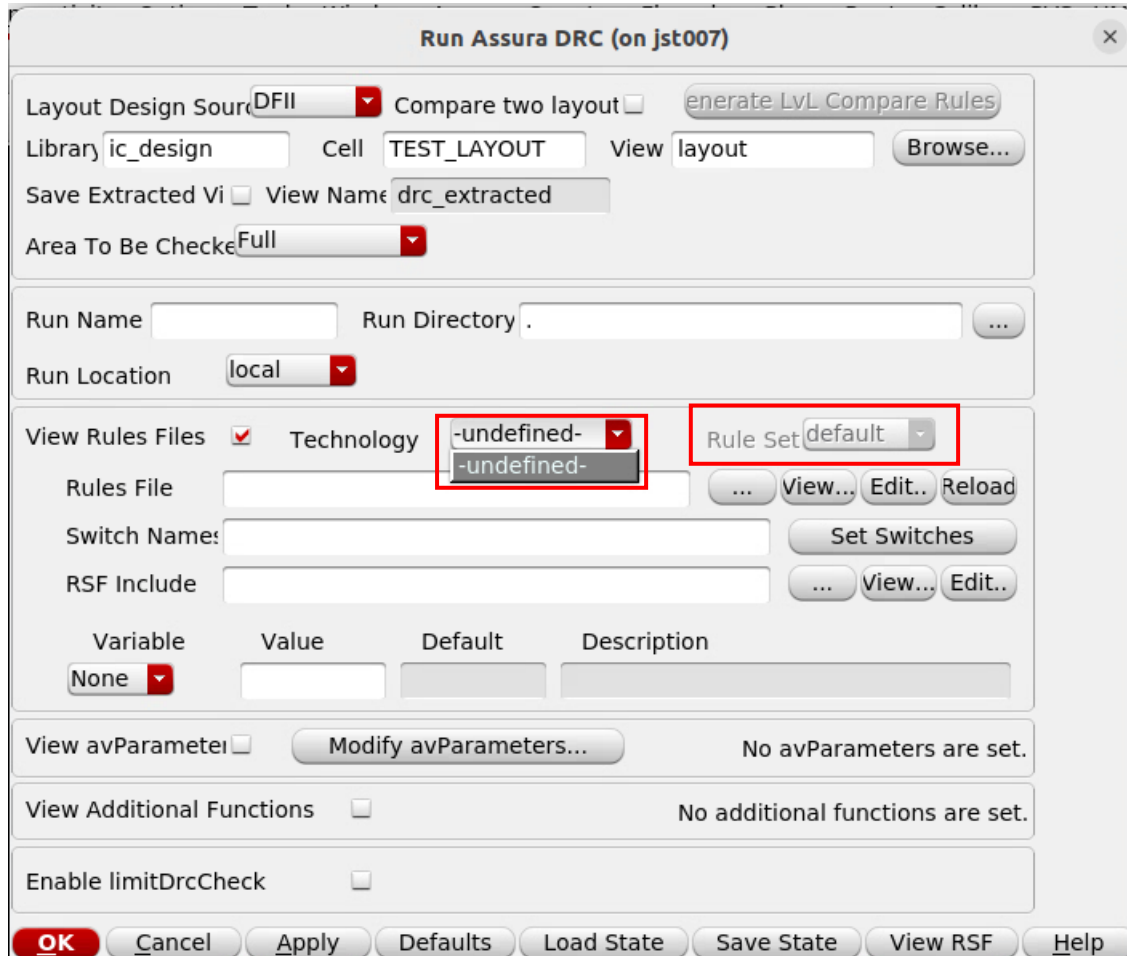


Voila! 🙌 🎉

Don't relax yet 😊. We still have some work to do to get things up and running 🏃.

## 2. Task 2: Fixing the Assura Rule Deck

Once you try to run DRC using Assura, you will notice that there is no “**UMC\_18\_CMOS**” option to choose in “**Technology**” and that the “**Rule Set**” option is greyed out.



To fix this, carry out the following steps:

- i. In `~/UMC_180NM_WORKSPACE/CDS_VISO` folder, create a file named “**assura\_tech.lib**” with contents as shown below:

```
EDARHEL7[tharakan@jst007 CDS_VISO]$ pwd
/home/tharakan/UMC_180NM_WORKSPACE/CDS_VISO
EDARHEL7[tharakan@jst007 CDS_VISO]$ gedit assura_tech.lib
```

```
*assura_tech.lib
~/UMC_180NM_WORKSPACE/CDS_VISO
DEFINE UMC_18_CMOS ./RuleDecks_Edit/Assura
```

Save the changes by hitting **Ctrl+S** and then close the “**assura\_tech.lib**” file.

- ii. In `~/UMC_180NM_WORKSPACE/CDS_VISO` folder, create a new folder named **“RuleDecks\_Edit”** (as shown below). In **RuleDecks\_Edit**, create a sub-folder **“Assura”**. This folder will house the edited rule files that we will use for DRC and LVS.

```
tharakan@jst007 CDS_VISO$ pwd
/home/tharakan/UMC_180NM_WORKSPACE/CDS_VISO
tharakan@jst007 CDS_VISO$ mkdir RuleDecks_Edit
tharakan@jst007 CDS_VISO$ cd RuleDecks_Edit/
tharakan@jst007 RuleDecks_Edit$ pwd
/home/tharakan/UMC_180NM_WORKSPACE/CDS_VISO/RuleDecks_Edit
tharakan@jst007 RuleDecks_Edit$ mkdir Assura
tharakan@jst007 RuleDecks_Edit$
```

- iii. Create a sub-directory **“DRC”** in the **“Assura”** folder and copy all the files from `~/UMC_180NM_WORSPACE/CDS_VISO/RuleDecks/Assura/G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-MMC-Assura-drc-2.11-p2` to this folder as shown below:

```
tharakan@jst007 Assura$ pwd
/home/tharakan/UMC_180NM_WORKSPACE/CDS_VISO/RuleDecks_Edit/Assura
tharakan@jst007 Assura$ mkdir DRC
tharakan@jst007 Assura$ cd DRC/
tharakan@jst007 DRC$ cp -RfL ../../../../RuleDecks/Assura/G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-MMC-Assura-drc-2.11-p2/* ./
tharakan@jst007 DRC$ ls
check_list.lst                               G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-MMC-Assura-drc-2.11-p2.rsf  umc_ant_assura_all_2.rsf
G-DF-GENERATION18-LOGO-Assura-drc-2.3-P1.rul  G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-MMC-Assura-drc-2.11-p2.rul  umc_ant_assura_all_2.rul
G-DF-LOGIC18-1.8V-3.3V-1P6M-Assura-drc-memory.rul  Release_notes
```

Verify the copy operation was successful by running **“ls”** as shown above.

- iv. Now we need to edit the file **“G-DF-MIXEDMODE\_RFCMOS18-1.8V-3.3V-1P6M-MMC-Assura-drc-2.11-p2.rul”** in the **DRC** folder. This is because this file contains reference to two other files using relative path which somehow causes issues with the Assura tool. We will modify these paths to absolute paths instead of relative paths. Open this file as shown below:

```
tharakan@jst007 DRC$ gedit G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-MMC-Assura-drc-2.11-p2.rul &
```

Scroll to the bottom of this file. You will notice the relative references there as shown below:

```
fat_met3_a = geomSize(fat_met3 2)
fat_met3_247 = geomSize( fat_met3_a 247)
m3_max_space_viol=geomAndNot(bulk_with_m3 fat_met3_247 )
m3_max_space_vio_a = geomSize(m3_max_space_viol 1)
m3_max_space_vio = geomSize(m3_max_space_vio_a 249)
errorLayer( m3_max_space_vio
  "4.24C: Maximum Metal3 to Metal3 spacing is 500um" )
); end of if switch for "metal2_is_top" or "metal3_is_top"

if( avSwitch( "metal2_is_top" ) || avSwitch( "metal3_is_top" ) ||
avSwitch( "metal4_is_top" )
  then
  else
  bulk_with_m4=geomButtOrOver( chip_ext ME4 keep>=2)
  fat_met4 = geomSize(ME4 1)
  fat_met4_a = geomSize(fat_met4 2)
  fat_met4_247 = geomSize( fat_met4_a 247)
  m4_max_space_viol=geomAndNot(bulk_with_m4 fat_met4_247 )
  m4_max_space_vio_a = geomSize(m4_max_space_viol 1)
  m4_max_space_vio = geomSize(m4_max_space_vio_a 249)
  errorLayer( m4_max_space_vio
    "4.26C: Maximum Metal4 to Metal4 spacing is 500um" )
  ); end of if switch for "metal2_is_top" or "metal3_is_top" or "metal4_is_top"

if( avSwitch( "metal2_is_top" ) || avSwitch( "metal3_is_top" ) ||
avSwitch( "metal4_is_top" ) || avSwitch( "metal5_is_top" ) then
  else
  bulk_with_m5=geomButtOrOver( chip_ext ME5 keep>=2)
  fat_met5 = geomSize(ME5 1)
  fat_met5_a = geomSize(fat_met5 2)
  fat_met5_247 = geomSize( fat_met5_a 247)
  m5_max_space_viol=geomAndNot(bulk_with_m5 fat_met5_247 )
  m5_max_space_vio_a = geomSize(m5_max_space_viol 1)
  m5_max_space_vio = geomSize(m5_max_space_vio_a 249)
  errorLayer( m5_max_space_vio
    "4.28C: Maximum Metal5 to Metal5 spacing is 500um" )
  ); end of if switch for "metal2_is_top" or "metal3_is_top" or "metal4_is_top" or
"metal5_is_top"

); end if "check_max_metal_space"

load( './G-DF-LOGIC18-1.8V-3.3V-1P6M-Assura-drc-memory.rul' )
load( './G-DF-GENERATION18-LOGO-Assura-drc-2.3-P1.rul' )
); drcExtractRules complete
```

Fix with absolute paths as shown below:

```

Open  [icon] G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-MMC-Ass... Save [icon] - [icon] x
~/UMC_180NM_WORKS...s_Edit/Assura/DRC
m3_max_space_viol=geomAndNot(bulk_with_m3 fat_met3_247 )
m3_max_space_vio_a = geomSize(m3_max_space_viol 1)
m3_max_space_vio = geomSize(m3_max_space_vio_a 249)
errorLayer( m3_max_space_vio
  "4.24C: Maximum Metal3 to Metal3 spacing is 500um" )
); end of if switch for "metal2_is_top" or "metal3_is_top"

  if( avSwitch( "metal2_is_top" ) || avSwitch( "metal3_is_top" ) ||
avSwitch( "metal4_is_top" )
  then
  else
  bulk_with_m4=geomButtOrOver( chip_ext ME4 keep>=2)
  fat_met4 = geomSize(ME4 1)
  fat_met4_a = geomSize(fat_met4 2)
  fat_met4_247 = geomSize( fat_met4_a 247)
  m4_max_space_viol=geomAndNot(bulk_with_m4 fat_met4_247 )
  m4_max_space_vio_a = geomSize(m4_max_space_viol 1)
  m4_max_space_vio = geomSize(m4_max_space_vio_a 249)
  errorLayer( m4_max_space_vio
    "4.26C: Maximum Metal4 to Metal4 spacing is 500um" )
  ); end of if switch for "metal2_is_top" or "metal3_is_top" or "metal4_is_top"

  if( avSwitch( "metal2_is_top" ) || avSwitch( "metal3_is_top" ) ||
avSwitch( "metal4_is_top" ) || avSwitch( "metal5_is_top" ) then
  else
  bulk_with_m5=geomButtOrOver( chip_ext ME5 keep>=2)
  fat_met5 = geomSize(ME5 1)
  fat_met5_a = geomSize(fat_met5 2)
  fat_met5_247 = geomSize( fat_met5_a 247)
  m5_max_space_viol=geomAndNot(bulk_with_m5 fat_met5_247 )
  m5_max_space_vio_a = geomSize(m5_max_space_viol 1)
  m5_max_space_vio = geomSize(m5_max_space_vio_a 249)
  errorLayer( m5_max_space_vio
    "4.28C: Maximum Metal5 to Metal5 spacing is 500um" )
  ); end of if switch for "metal2_is_top" or "metal3_is_top" or "metal4_is_top" or
"metal5_is_top"|

) ; end if "check_max_metal_space"

load( "/dkits/umc/180nm/msrf180/pdk_b02pb/RuleDecks/Assura/G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-
MMC-Assura-drc-2.11-p2/G-DF-LOGIC18-1.8V-3.3V-1P6M-Assura-drc-memory.rul" )
load( "/dkits/umc/180nm/msrf180/pdk_b02pb/RuleDecks/Assura/G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-
MMC-Assura-drc-2.11-p2/G-DF-GENERATION18-LOGO-Assura-drc-2.3-P1.rul" )
); drcExtractRules complete

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```

Please note that each load statement is on a single line. **Save the changes by hitting Ctrl+S** and then close the file.

We have successfully fixed the rule deck for DRC. Now, let us do the same for the LVS rule deck.

- v. Create a folder named "LVS" in the folder  
~/UMC\_180NM\_WORKSPACE/CDS\_VISO/RuleDecks\_Edit/Assura as shown below:

```

tharakan@jed1:~
EDARHEL7[tharakan@jst092 DRC]$ pwd
/home/tharakan/UMC_180NM_WORKSPACE/CDS_VISO/RuleDecks_Edit/Assura/DRC
EDARHEL7[tharakan@jst092 DRC]$ cd ..
EDARHEL7[tharakan@jst092 Assura]$ pwd
/home/tharakan/UMC_180NM_WORKSPACE/CDS_VISO/RuleDecks_Edit/Assura
EDARHEL7[tharakan@jst092 Assura]$ mkdir LVS

```

- vi. Now copy the files from  
**~/UMC\_180NM\_WORSPACE/CDS\_VISO/RuleDecks/Assura/G-DF-MIXED\_MODE\_RFCMOS18-1.8V\_3.3V-1P6M-MMC\_ASSURA-LVS-2.1-P2** as shown below:

```
EDARHEL7[tharakan@jst092 Assura]$ cd LVS/
EDARHEL7[tharakan@jst092 LVS]$ cp -RfL ../../RuleDecks/Assura/G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2/* ./
EDARHEL7[tharakan@jst092 LVS]$ ls
G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2-COMPARE.RUL  G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2-RSF
G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2-EXTRACT.RUL
```

Verify the copy operation was successful by running “ls” as shown above.

- vii. We need to create one more file. It is the last one – surely! 😊 Go back to the Assura folder and create a file “**techRuleSets**” with contents as shown below:

```
tharakan@jed1:~
EDARHEL7[tharakan@jst092 LVS]$ pwd
/home/tharakan/UMC_180NM_WORKSPACE/CDS_VISO/RuleDecks_Edit/Assura/LVS
EDARHEL7[tharakan@jst092 LVS]$ cd ..
EDARHEL7[tharakan@jst092 Assura]$ pwd
/home/tharakan/UMC_180NM_WORKSPACE/CDS_VISO/RuleDecks_Edit/Assura
EDARHEL7[tharakan@jst092 Assura]$ gedit techRuleSets &
```

```
techRuleSets
~/UMC_180NM_WORKSPACE/CDS_VISO/RuleDecks_Edit/Assura

ruleSet( "DRC"
(DrcRules ". /DRC/G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-MMC-Assura-drc-2.11-p2.rul")
)
ruleSet( "LVS"
(LvsExtractRules ". /LVS/G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2-EXTRACT.RUL" )
(LvsCompareRules ". /LVS/G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2-COMPARE.RUL" )
)
```

**Save the changes by hitting Ctrl+S** and then close the file.

- viii. Now back to the virtuoso layout window. Click on Assura -> Technology. Make sure it points to the “**assura\_tech.lib**” file we created in step (i).

