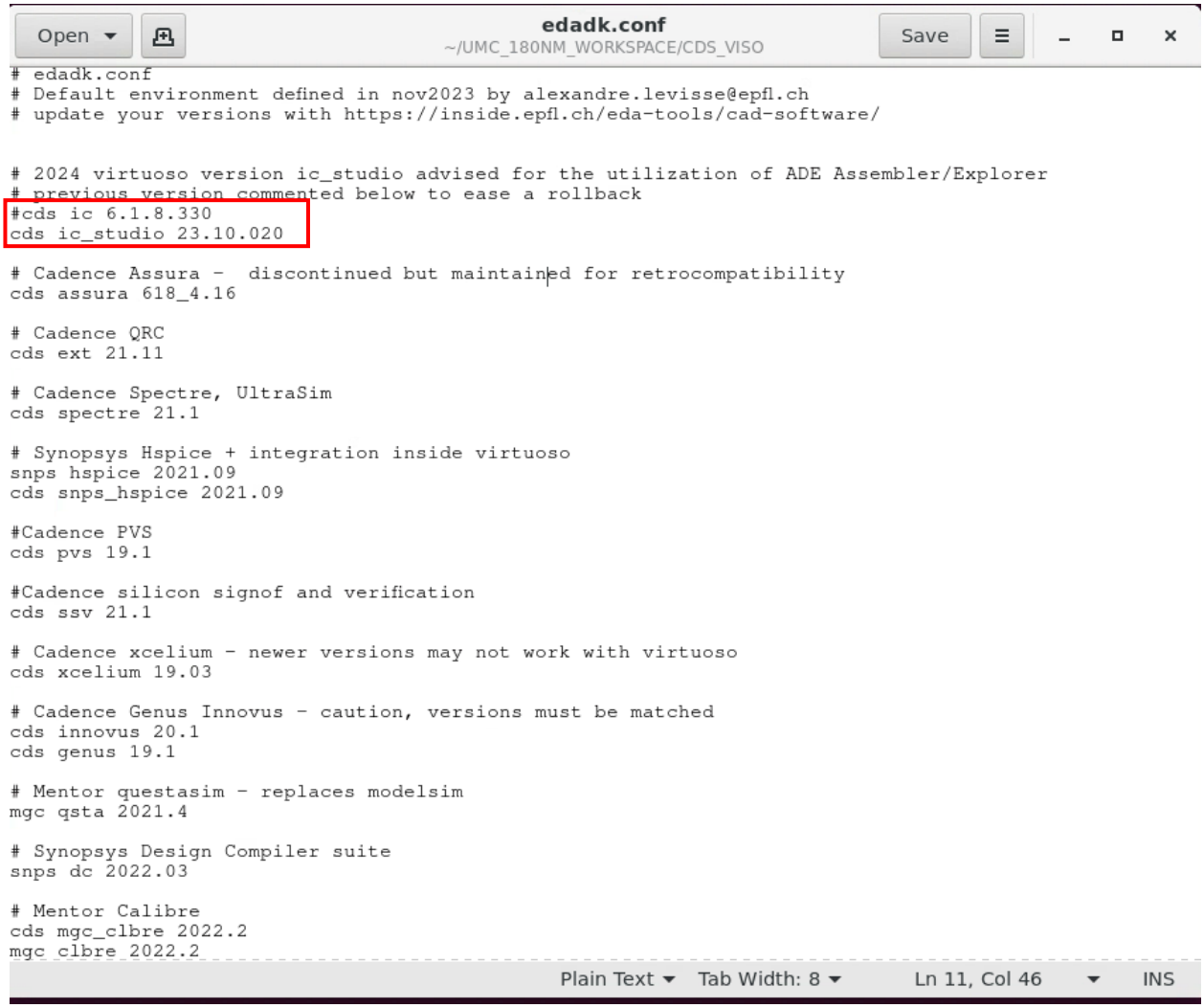
Fixing Assura for DRC and LVS (A mountain⛰️ to climb!)

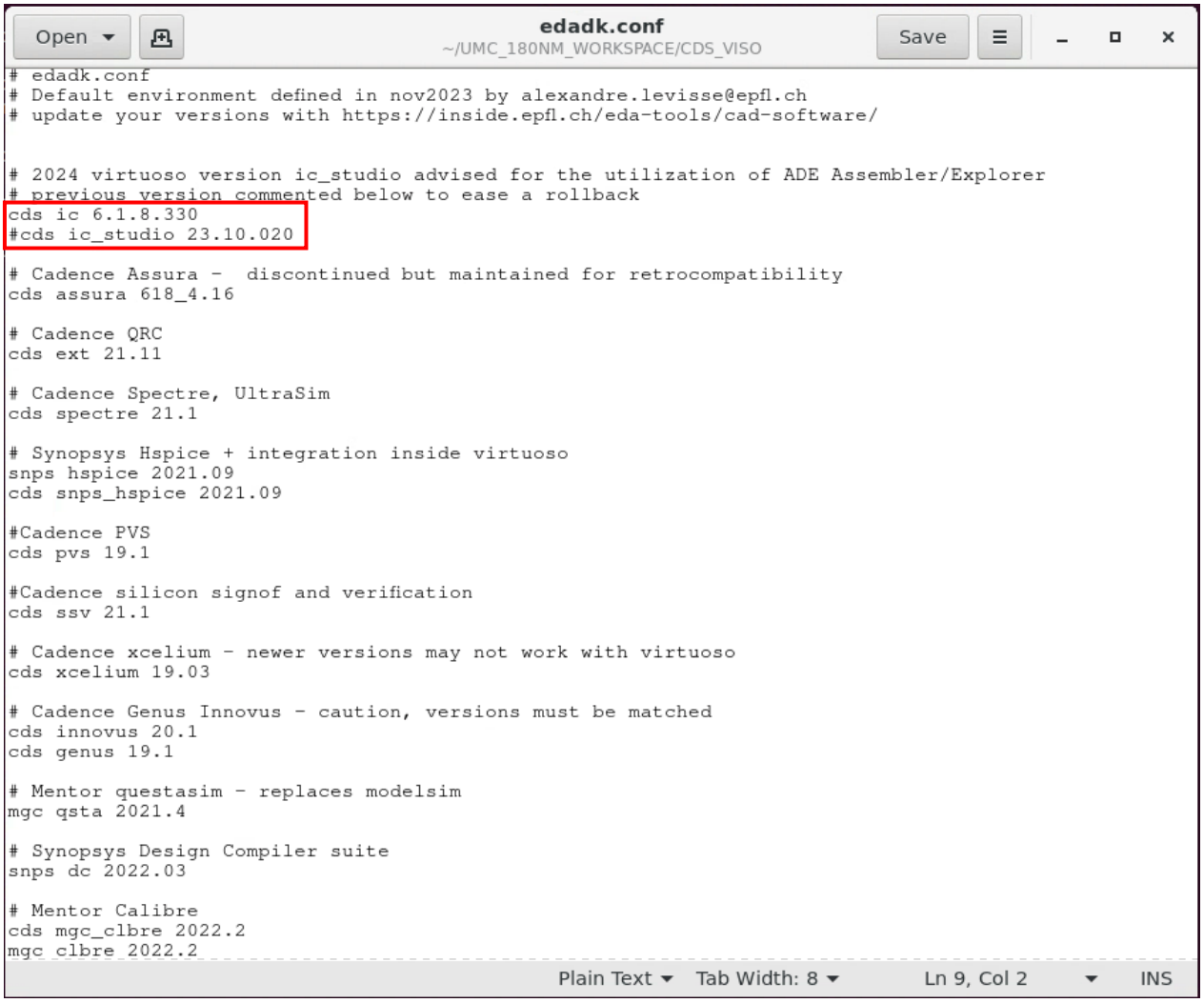
1. Task 1: Making Assura show up

By default, Assura does not show up in the latest version of Cadence Virtuoso (ic_studio 23.10.020). So, we will revert to an older version of virtuoso for this lab. To do this, close all your existing cadence virtuoso windows (do not disconnect from the **jed** machines though) and go to **UMC_180NM_WORKSPACE/CDS_VISO** folder and open the **edadk.conf** file as shown below:

In the edadk.conf file (shown below), you will notice that “cds ic 6.1.8.330” (older version of cadence virtuoso) is commented out and “cds ic_studio 23.10.020” (newer version of cadence virtuoso) is being used. We will comment out the newer version and use the older version for this TP. Don’t worry - you can continue to use the older version for all your TPs and homework 😊.

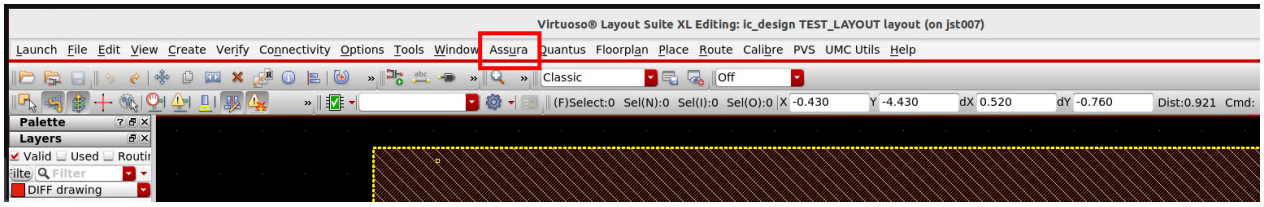


After making this change, your edadk.conf file should look something like this:



Save the changes by hitting Ctrl+S and then close the “edadk.conf” file.

Now, open virtuoso and in the layout window, you should be able to find Assura.

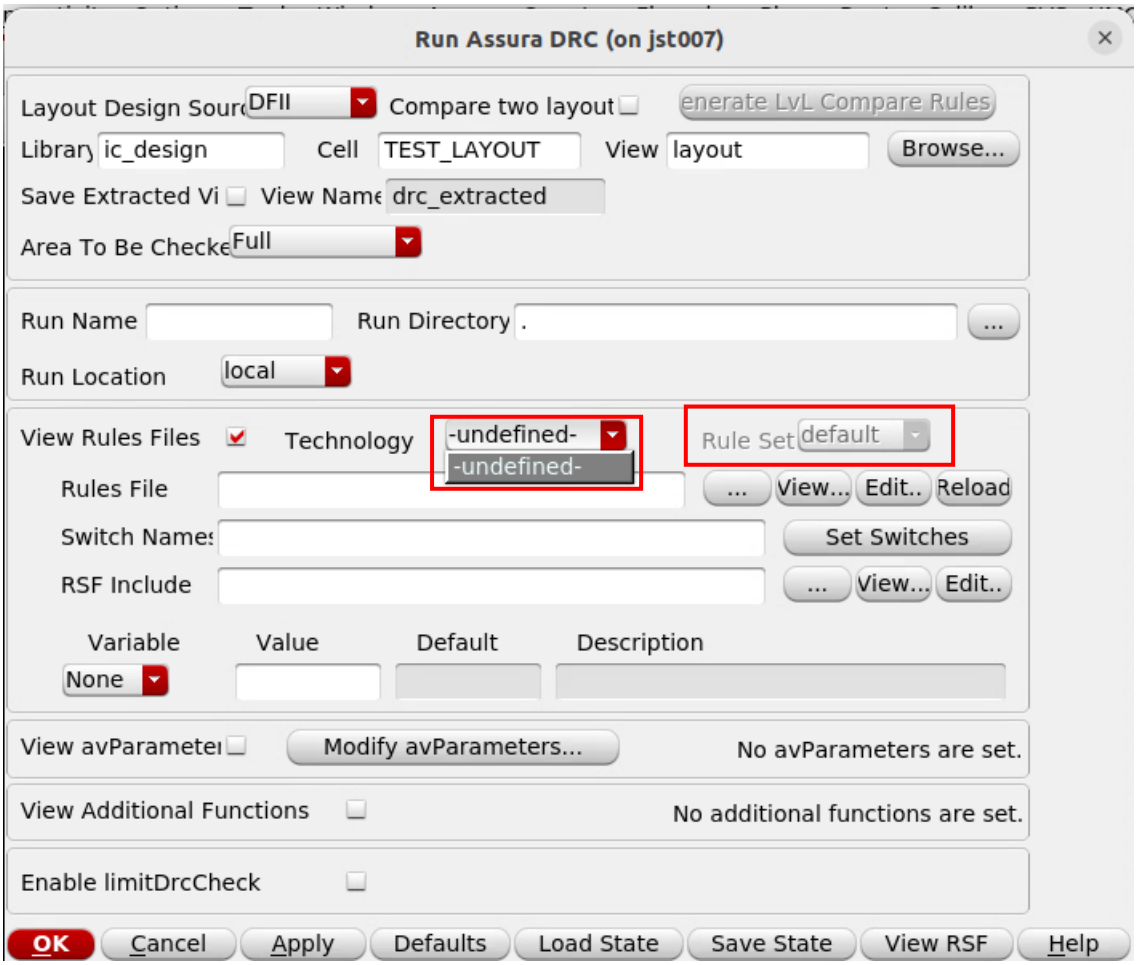


Voila! 🕺 💃

Don’t relax yet😊. We still have some work to do to get things up and running 🏃.

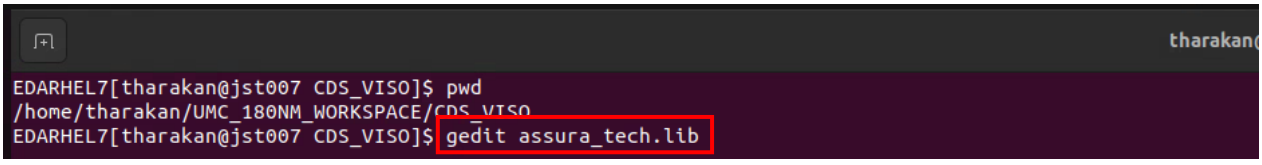
2. Task 2: Fixing the Assura Rule Deck

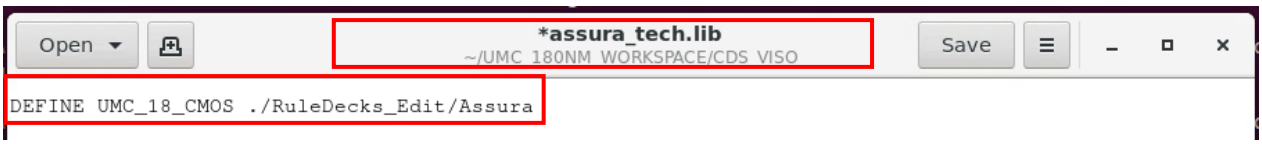
Once you try to run DRC using Assura, you will notice that the there is no "**UMC_18_CMOS**" option to choose in "**Technology**" and that the "**Rule Set**" option is greyed out.



To fix this, carry out the following steps:

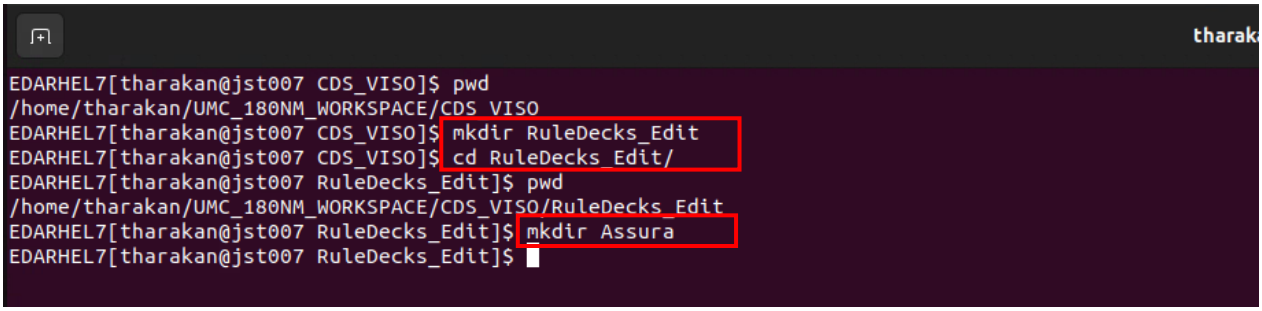
i. In ~/UMC_180NM_WORKSPACE/CDS_VISO folder, create a file named "**assura_tech.lib**" with contents as shown below:



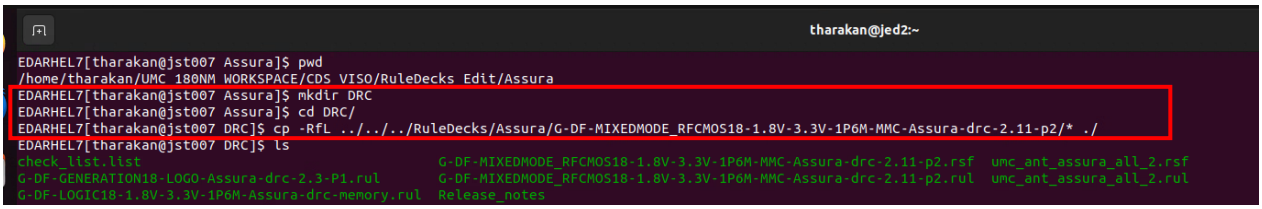


Save the changes by hitting Ctrl+S and then close the "**assura_tech.lib**" file.

ii. In ~/UMC_180NM_WORKSPACE/CDS_VISO folder, create a new folder named "**RuleDecks_Edit**" (as shown below). In **RuleDecks_Edit**, create a sub-folder "**Assura**". This folder will house the edited rule files that we will use for DRC and LVS.



iii. Create a sub-directory "**DRC**" in the "**Assura**" folder and copy all the files from **~/UMC_180NM_WORSPACE/CDS_VISO/RuleDecks/Assura/G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-MMC-Assura-drc-2.11-p2** to this folder as shown below:

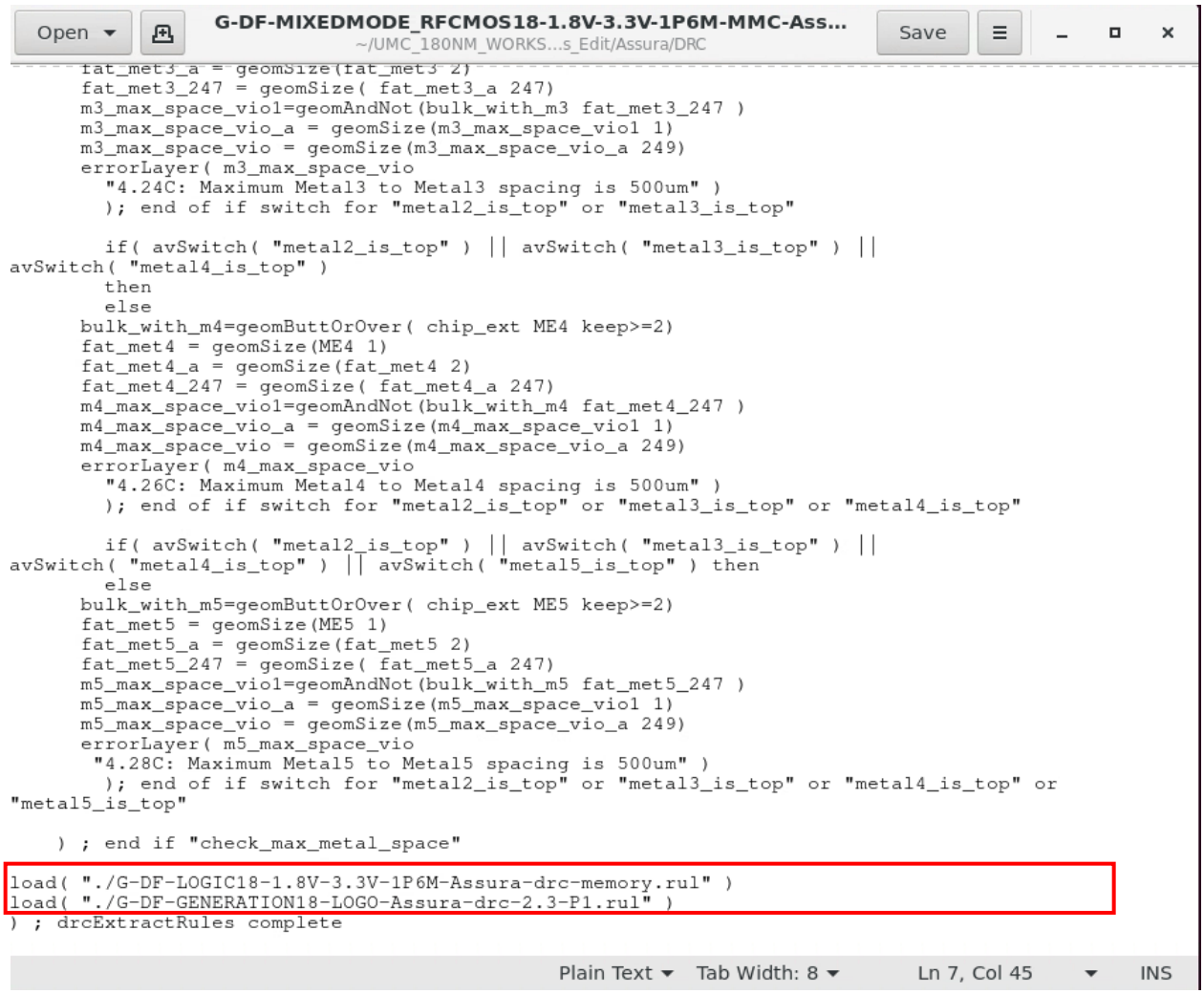


Verify the copy operation was successful by running "**ls**" as shown above.

iv. Now we need to edit the file "**G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-MMC-Assura-drc-2.11-p2.rul**" in the **DRC** folder. This is because this file contains reference to two other files using relative path which somehow causes issues with the Assura tool. We will modify these paths to absolute paths instead of relative paths. Open this file as shown below:

```
EDARHEL7[tharakan@jst007 DRC]$ gedit G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-MMC-Assura-drc-2.11-p2.rul &
```

Scroll to the bottom of this file. You will notice the relative references there as shown below:

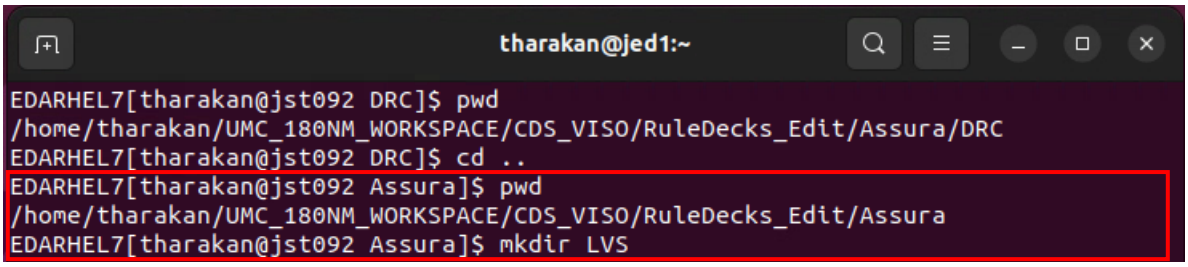


Fix with absolute paths as shown below:

Please note that each load statement is on a single line. **Save the changes by hitting Ctrl+S** and then close the file.

We have successfully fixed the rule deck for DRC. Now, let us do the same for the LVS rule deck.

v. Create a folder named “LVS” in the folder ~/UMC_180NM_WORKSPACE/CDS_VISO/RuleDecks_Edit/Assura as shown below:



vi. Now copy the files from **~/UMC_180NM_WORSPACE/CDS_VISO/RuleDecks/Assura/G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2** as shown below:

```
EDARHEL7[tharakan@jst092 Assura]$ cd LVS/
EDARHEL7[tharakan@jst092 LVS]$ cp -RfL ../../../RuleDecks/Assura/G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2/* ./
EDARHEL7[tharakan@jst092 LVS]$ ls
G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2-COMPARE.RUL  G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2.RSF
G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2-EXTRACT.RUL
```

Verify the copy operation was successful by running "**ls**" as shown above.

vii. We need to create one more file. It is the last one – surely! 😉 Go back to the Assura folder and create a file "**techRuleSets**" with contents as shown below:

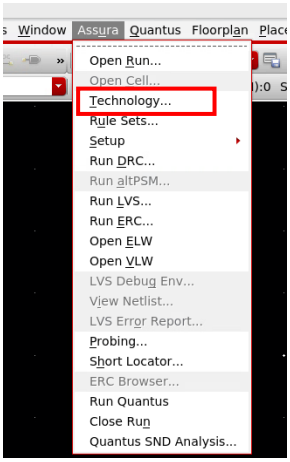
```
tharakan@jed1:~
EDARHEL7[tharakan@jst092 LVS]$ pwd
/home/tharakan/UMC_180NM_WORKSPACE/CDS_VISO/RuleDecks_Edit/Assura/LVS
EDARHEL7[tharakan@jst092 LVS]$ cd ..
EDARHEL7[tharakan@jst092 Assura]$ pwd
/home/tharakan/UMC_180NM_WORKSPACE/CDS_VISO/RuleDecks_Edit/Assura
EDARHEL7[tharakan@jst092 Assura]$ gedit techRuleSets &
```

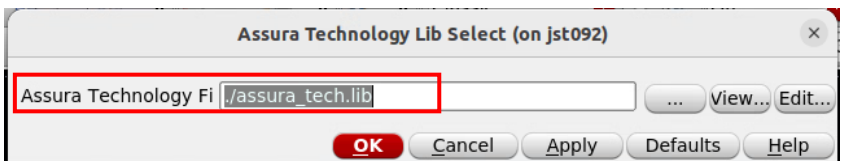
Open techRuleSets ~/UMC_180NM_WORKSPACE/CDS_VISO/RuleDecks_Edit/Assura

```
ruleSet( "DRC"
(DrcRules "./DRC/G-DF-MIXEDMODE_RFCMOS18-1.8V-3.3V-1P6M-MMC-Assura-drc-2.11-p2.rul")
)
ruleSet( "LVS"
     (LvsExtractRules      "./LVS/G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2-EXTRACT.RUL" )
     (LvsCompareRules      "./LVS/G-DF-MIXED_MODE_RFCMOS18-1.8V_3.3V-1P6M-MMC_ASSURA-LVS-2.1-P2-COMPARE.RUL" )
)
```

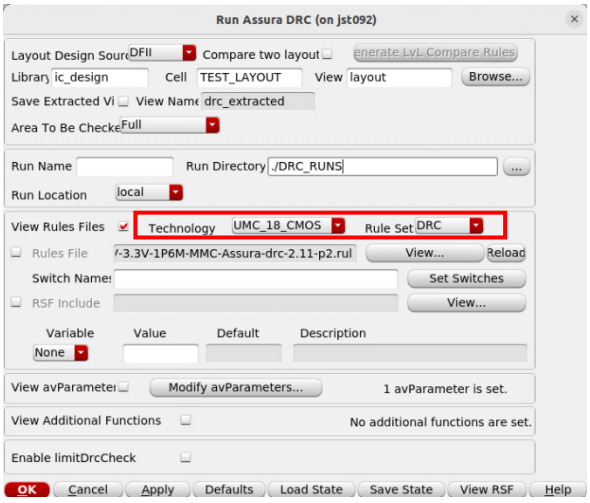
Save the changes by hitting Ctrl+S and then close the file.

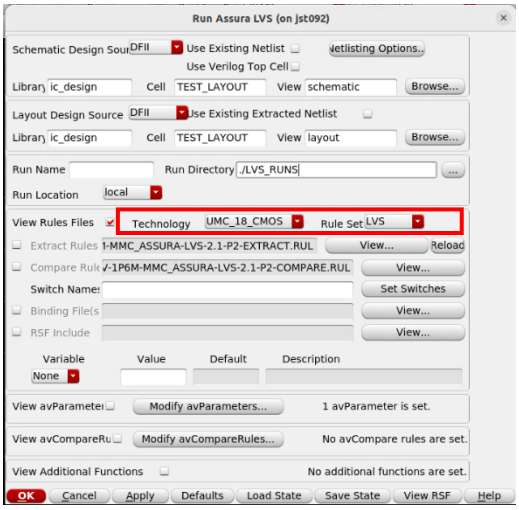
viii. Now back to the virtuoso layout window. Click on Assura -> Technology. Make sure it points to the "assura_tech.lib" file we created in step (i).





ix. Cheers! We are done with fixing the setup. Now you should be able to run DRC and LVS as described in TP-4.





Clarification: There was a change in our setup from last year. That is why you have to do these extra steps. Sorry about that. On the bright side – there is something to learn from everything! 😊